Ordering number: EN 1463C

Monolithic Linear IC

SANYO No.1463C

LA4265

3.5W Monaural Power Amp

Features

- Minimum number of external parts required (No input capacitor, bootstrap capacitor required)
- High output: 3.5 W typ (V_{CC} = 16 V, R_L = 8 Ω, THD = 10 %)
- Soft clip, causing little harmonic disturbance to radios
- Small pop noise at the time of power switch ON/OFF
- Built-in protector against abnormal modes (Thermal shutdown, overvoltage)

Maximum Ratings/T_a = 25°C

			unit
Maximum supply voltage	V_{CC} max	25	V
Maximum output current	I_o peak	2	A
Allowable power dissipation	P_d max	7.5*	W
Operating temperature	Topr	−20 ~ +75	°C
Storage temperature	T_{stg}	−40 ~ +150	°C

* With 100 x 120 x 1.5 mm³ A1 heat sink

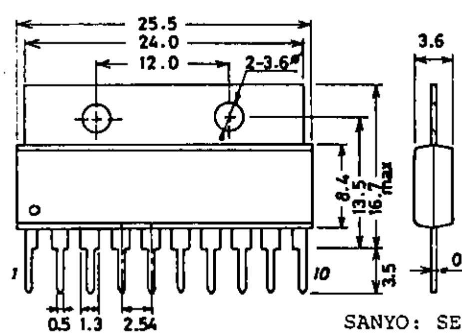
Operating Conditions/T_a = 25°C

			unit
Recommended supply voltage	V_{CC}	16	V
Recommended load resistance	R_L	8	Ω
Operating supply voltage range	V_{CC}	9 ~ 24	V

Operating Characteristics/T_a = 25°C, V_{CC} = 16V, R_L = 8Ω, f = 1 kHz, R_g = 600 Ω, See specified test circuit (based on sample application circuit).

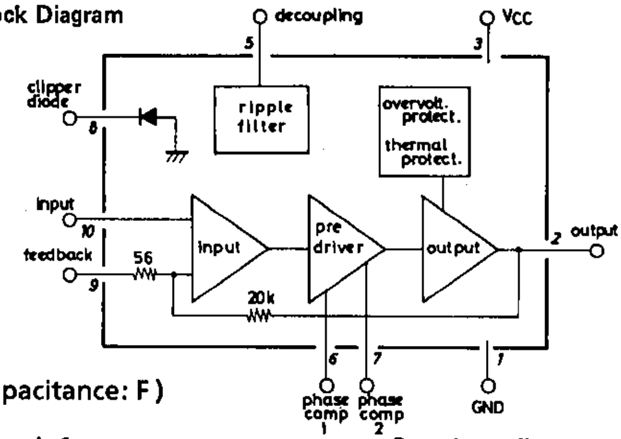
			min	typ	max	unit
Quiescent current	I_{CCO}			35	50	mA
Voltage gain	VG		48	50	52	dB
Output power	P_O	THD = 10 %	3.0	3.5		W
Total harmonic distortion	THD	P_O = 0.5 W		0.3	1.0	%
Output noise voltage	V_{NO}	R_g = 10 kΩ, BPF = 20 Hz to 20 kHz		0.65	1.5	mV
Ripple rejection	SVRR	R_g = 0, f_R = 100 Hz, V_R = 0.5 V	40	50		dB

Package Dimensions
(unit: mm)
3018A-S10FIC



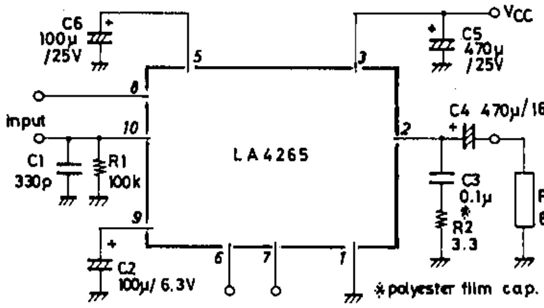
SANYO: SEP10F

Equivalent Circuit Block Diagram

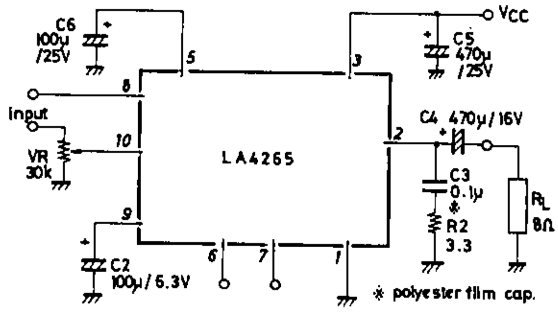


Unit (resistance: Ω, capacitance: F)

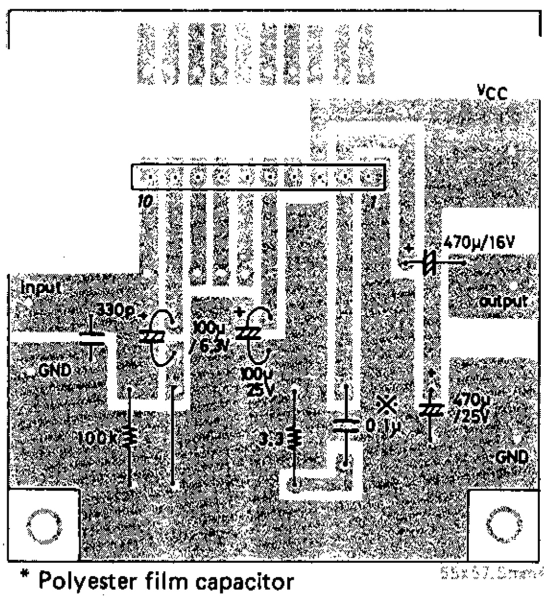
Sample application circuit 1
(Recommended circuit)



Sample application circuit 2 (Circuit with minimum number of external parts)

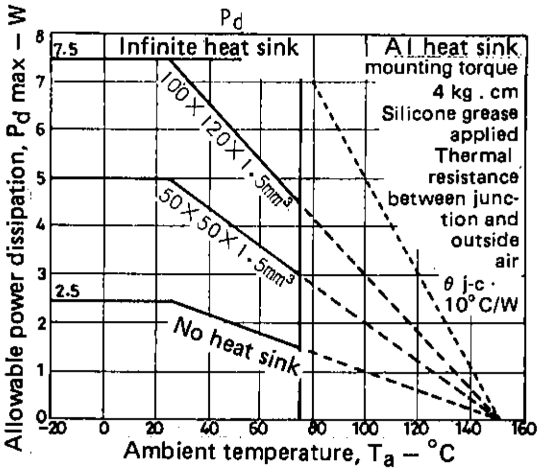


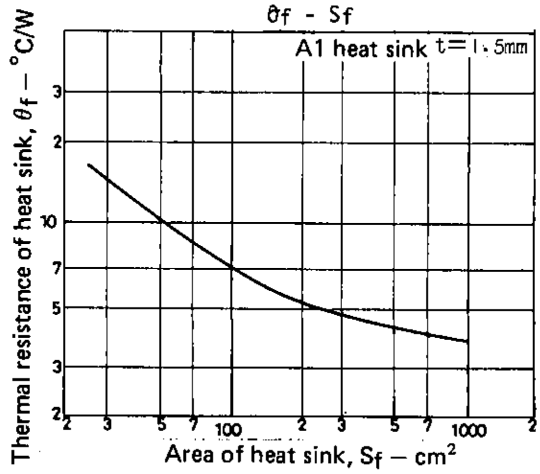
Sample printed circuit pattern



Cu-foiled area
55×57.5 mm2

* Polyester film capacitor





Description of External Parts

C_1 (330 pF) : Input short capacitor
Reduces the high frequency noise when the input impedance is increased. Not required when the input impedance is decreased.

C_2 (100 μF) : Feedback capacitor
Decreasing the capacitance value lowers the low frequency response. Increasing the capacitance value makes the starting time later.

C_3 (0.1 μF polyester film capacitor) : Oscillation blocking capacitor
Decreasing the capacitance value causes oscillation to occur easily. Use a polyester film capacitor that is good in high frequency response and temperature characteristic. The use of an electrolytic capacitor may cause oscillation to occur at low temperatures.

C_4 (470 μF) : Output capacitor
Decreasing the capacitance value causes insufficient power at low frequencies.

C_5 (470 μF) : Power capacitor
Decreasing the capacitance value causes ripple to occur easily. Locating at a distance from the IC or removing this capacitor may cause oscillation to occur.

C_6 (100 μF) : Ripple filter capacitor
Decreasing the capacitance value excessively or removing this capacitor causes ripple to occur. However, increasing the capacitance value does not always cause ripple to be reduced. Decreasing the capacitance value makes the starting time earlier.

R_1 (100 kΩ) : Input bias resistor
Determines the bias (bias of zero potential) to be applied to the input pin and the input impedance. Not required if a variable resistor is also used as this resistor.

R_2 (3.3 Ω) : Resistor connected in series with oscillation blocking capacitor
Prevents phase shift attributable to the oscillation blocking capacitor so that oscillation is hard to occur.

Note for Changing Voltage Gain

The voltage gain can be reduced by adding an external resistor (R_{NF}) in series with the feedback capacitor. (See V_G-R_{NF} characteristic curve.) However, it should be noted that various characteristics are also changed (THD-V_G, V_{NO}-V_G, Vro-V_G). The voltage gain must not be reduced to be less than 30 dB. Since the frequency response is extended and oscillation is liable to occur when the voltage gain is reduced, high-cut must be made as required. (High-cut is made by connecting a capacitor of approximately 30 pF across pins (6) and (7).)

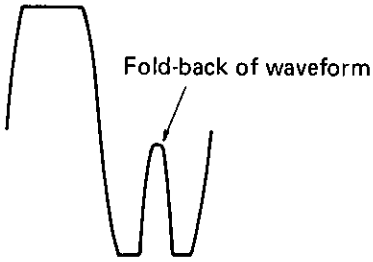
External Muting

If external muting is required, make the circuit as shown on next page. In this case, the pop noise is similar to that which occurs at the time of power switch ON/OFF. If the value of the series resistor is decreased, more pop noise is heard at the time of attack; if increased, muting is hard to work.

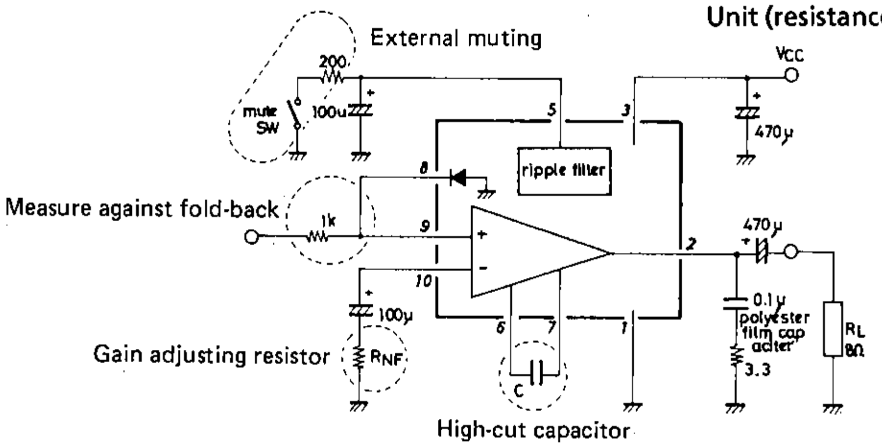
Measure against Fold-back of Output Waveform

Since the input pin is zero-biased, the circuit may be saturated at an overinput, causing a part of the output waveform to be folded back (e.g. when the peak input voltage exceeds 600 mV). In such a case, the fold-back of the waveform can be prevented by using the built-in diode (also can be prevented by using an external diode). When the built-in diode is used, a resistor must be connected in series with the input pin to cause the diode to conduct no overcurrent (10 mA or less).

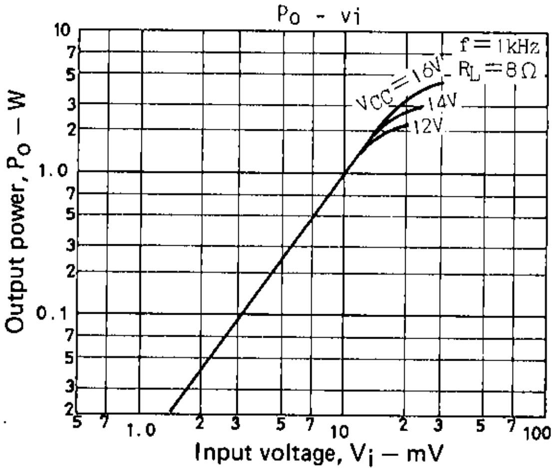
Fold-back of Output Waveform



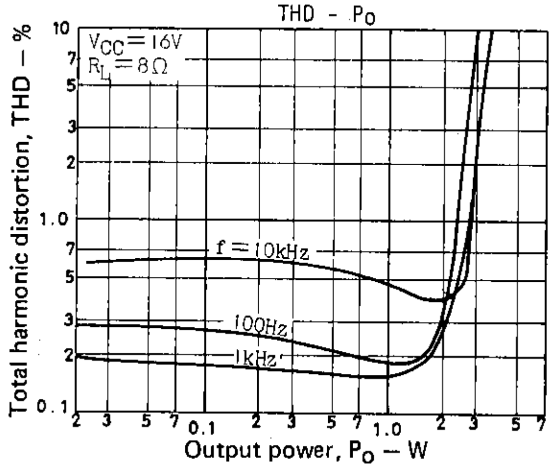
Unit (resistance: Ω, capacitance: F)



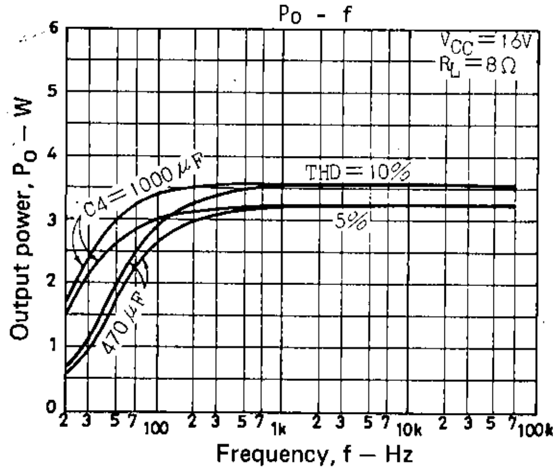
Po - vi



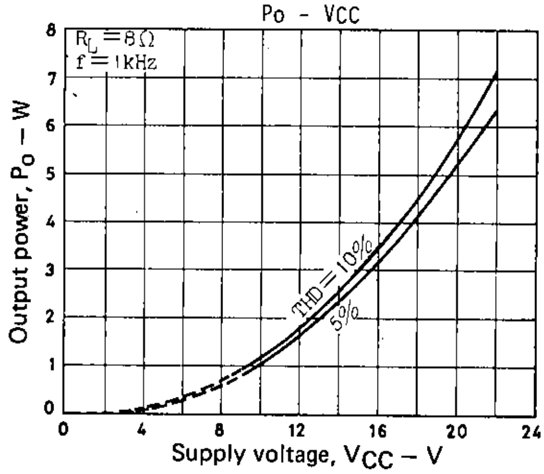
THD - Po



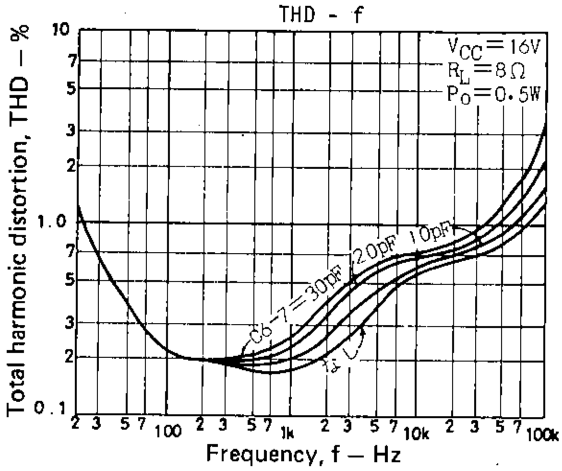
Po - f



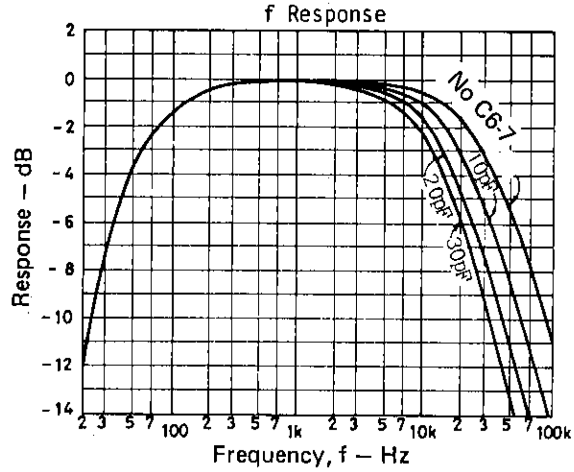
Po - VCC



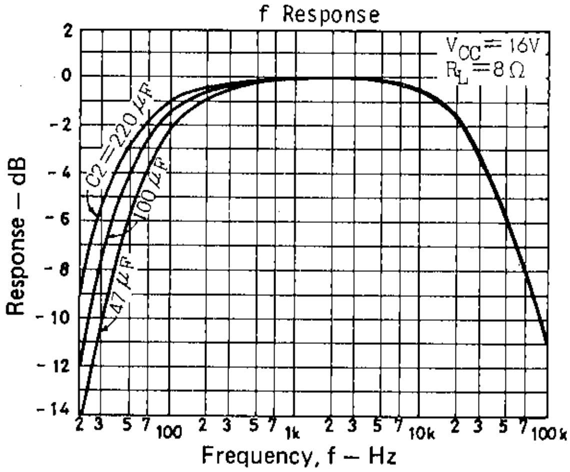
THD - f



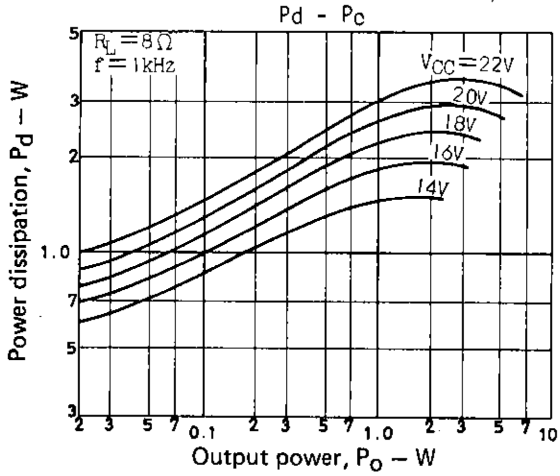
f Response



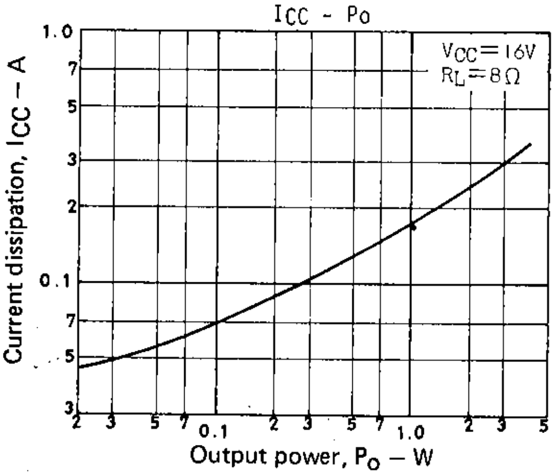
f Response



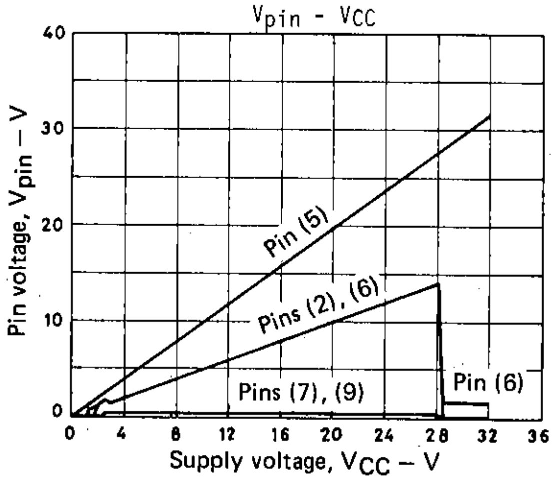
Pd - Pc



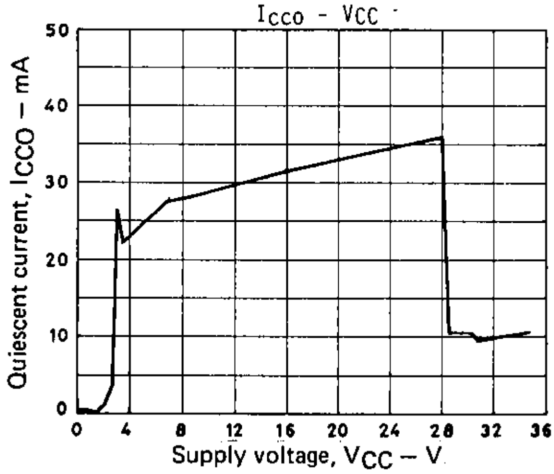
ICC - Po



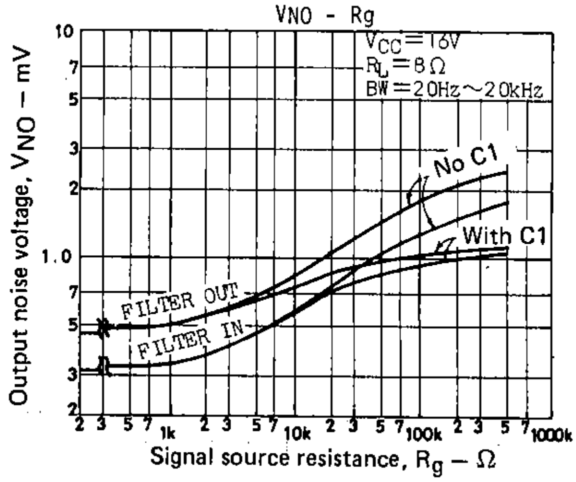
Vpin - VCC

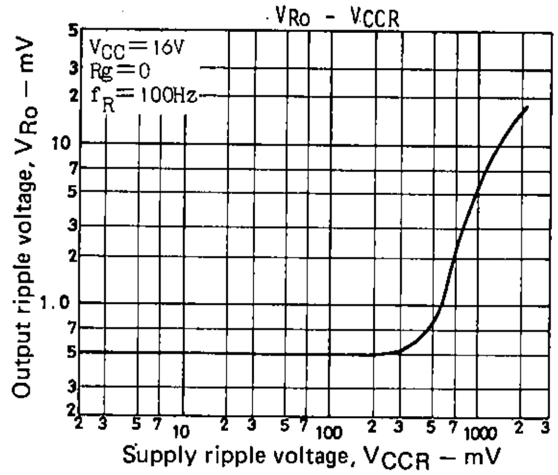


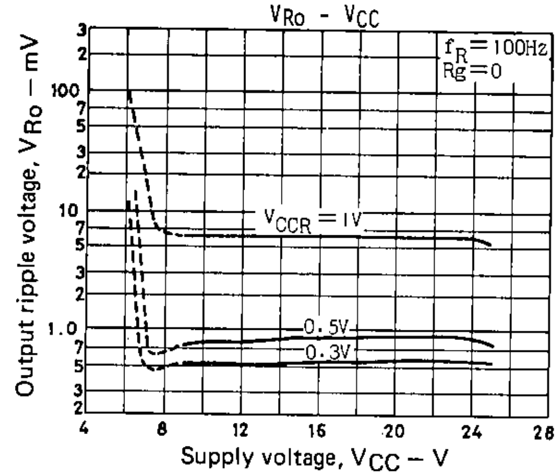
Icco - VCC

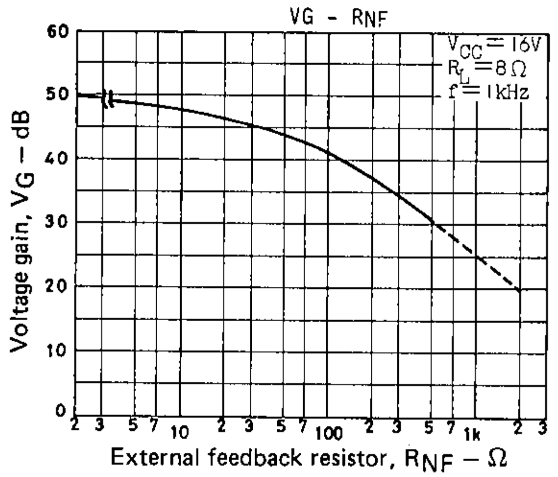


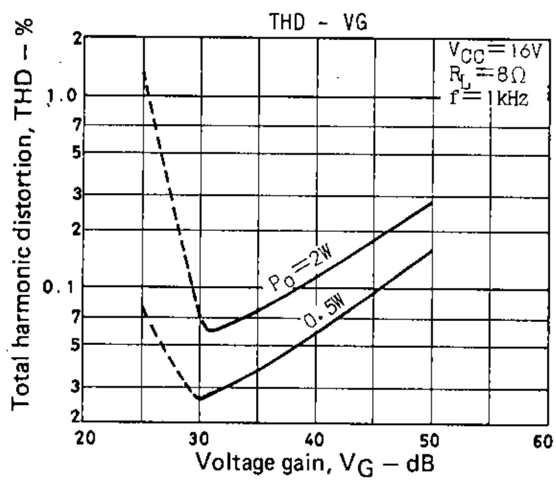
VNO - Rg

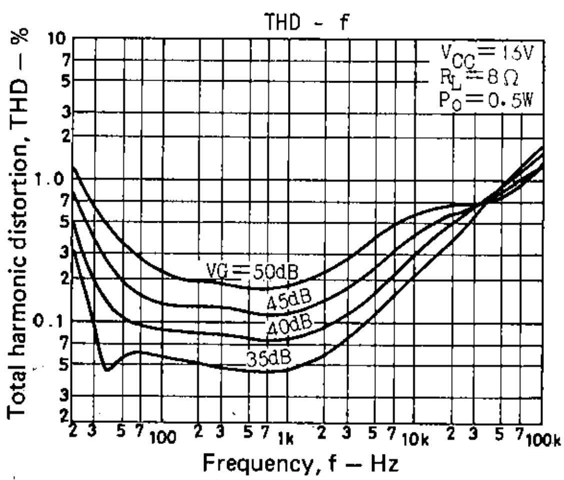


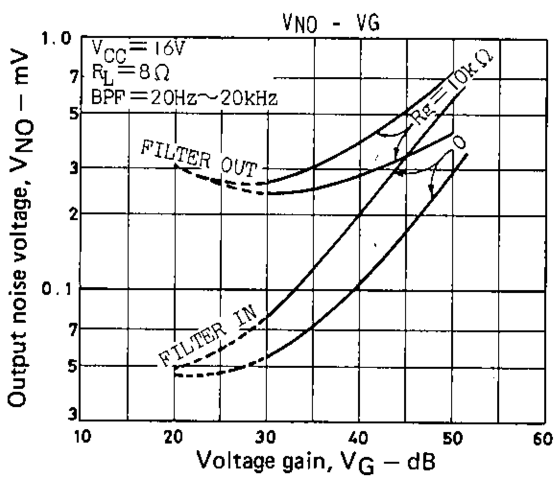

VRo - VCCR
VCC=16V
Rg=0
fR=100Hz
Output ripple voltage, VRo – mV
Supply ripple voltage, VCCR – mV

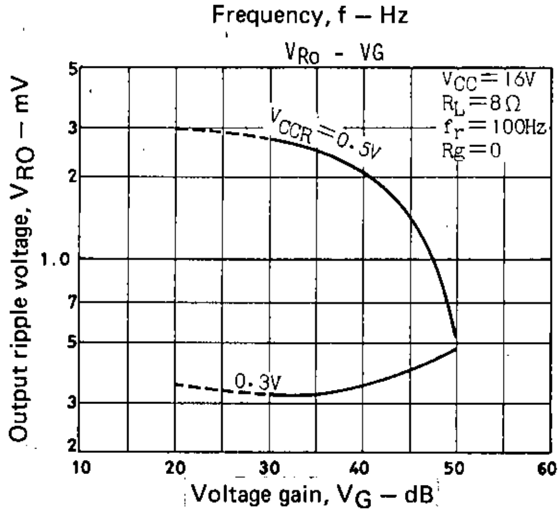

VRo - VCC
fR=100Hz
Rg=0
VCCR=1V
0.5V
0.3V
Output ripple voltage, VRo – mV
Supply voltage, VCC – V

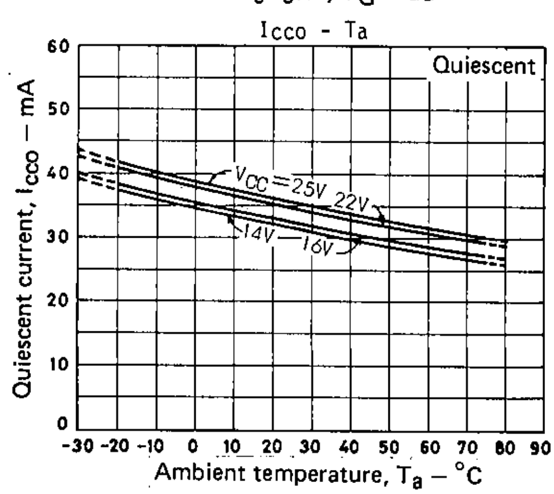

VG - RNF
VCC=16V
RL=8Ω
f=1kHz
Voltage gain, VG – dB
External feedback resistor, RNF – Ω

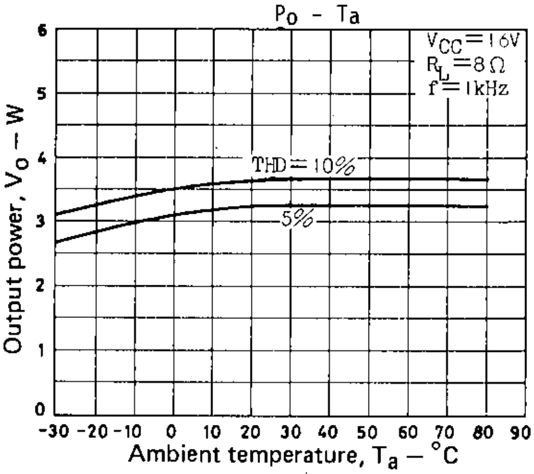

THD - VG
VCC=16V
RL=8Ω
f=1kHz
Po=2W
0.5W
Total harmonic distortion, THD – %
Voltage gain, VG – dB

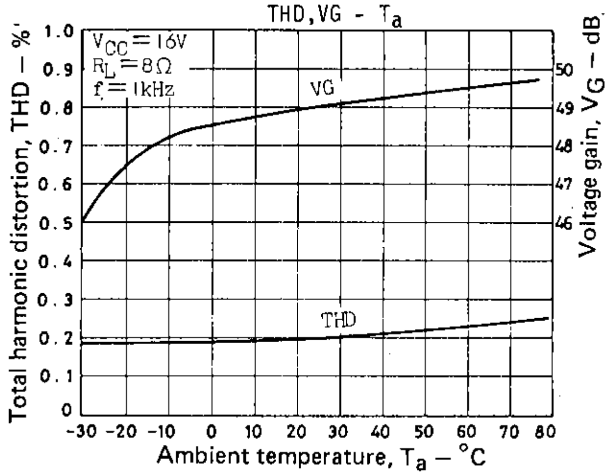

THD - f
VCC=16V
RL=8Ω
Po=0.5W
VG=50dB
45dB
40dB
35dB
Total harmonic distortion, THD – %
Frequency, f – Hz


VNO - VG
VCC=16V
RL=8Ω
BPF=20Hz~20kHz
FILTER OUT
FILTER IN
Rg=10kΩ
0
Output noise voltage, VNO – mV
Voltage gain, VG – dB

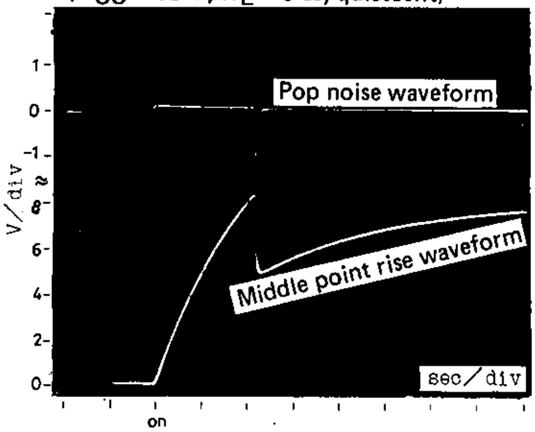

VRo - VG
VCC=16V
RL=8Ω
fr=100Hz
Rg=0
VCCR=0.5V
0.3V
Output ripple voltage, VRO – mV
Voltage gain, VG – dB


Icco - Ta
Quiescent
VCC=25V
22V
14V
16V
Quiescent current, Icco – mA
Ambient temperature, Ta – °C

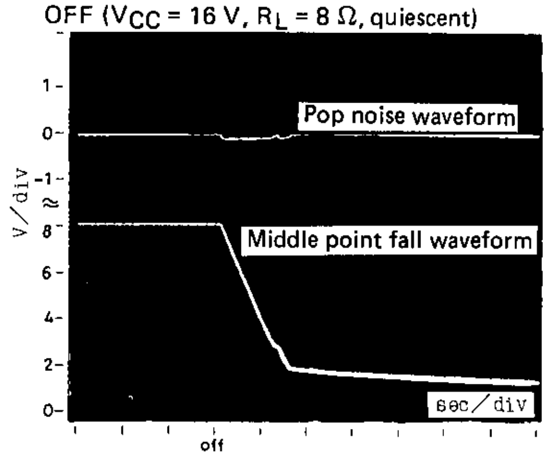




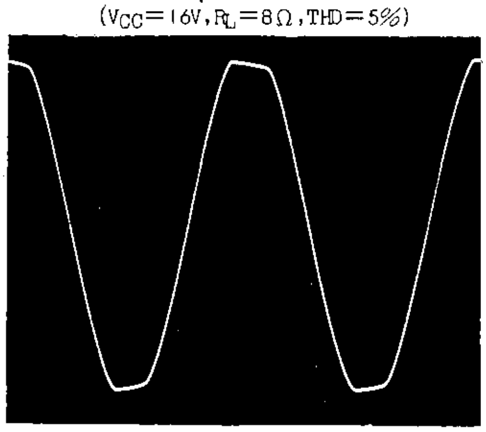
Pop noise waveform at the time of power switch ON (V_{CC} = 16 V, R_L = 8 Ω, quiescent)



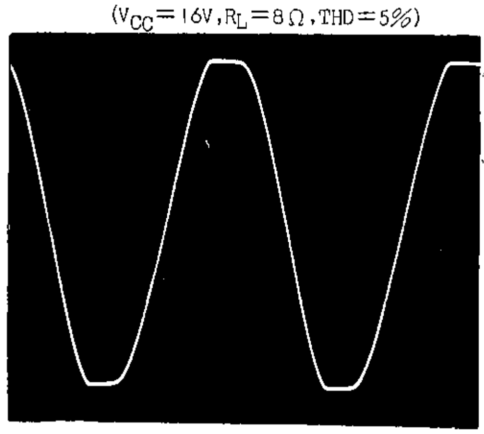
Pop noise waveform at the time of power switch OFF (V_{CC} = 16 V, R_L = 8 Ω, quiescent)



f = 1 kHz clip waveform
(V_{CC}=16V, R_L=8Ω, THD=5%)



f = 10 kHz clip waveform
(V_{CC}=16V, R_L=8Ω, THD=5%)



Proper Cares in Using IC

- Maximum ratings
  If the IC is used in the vicinity of the maximum ratings, even a slight variation in conditions may cause the maximum ratings to be exceeded, thereby leading to breakdown. Allow an ample margin of variation for supply voltage, etc. and use the IC in the range where the maximum ratings are not exceeded.

- Pin-to-pin short
  If power is applied when the space between pins is shorted, breakdown or deterioration may occur. When mounting the IC on the board or applying power, make sure that the space between pins is not shorted with solder, etc.

- When used in radio applications
  When using in radios, allow a sufficient space between IC and bar antenna.

- Printed circuit pattern
  When designing the printed circuit pattern, make the power supply, output, and ground lines thick and short and arrange the pattern and parts so that no feedback loop is formed between input and output. Place power capacitor C5, oscillation blocking capacitor C3 as close to IC pins as possible to prevent oscillation from occurring. Refer to the sample printed circuit pattern.

- Some plug jacks to be used for connecting to the external speaker are such that both poles are short-circuited once when connecting. In this case, the load is short-circuited, which may break down the IC.